REMARKS

Claims 1-16 and 19-24 are all the claims pending in the application.

Claims 1-16 and 19-24 are rejected under 35 U.S.C. § 103(a). Applicant respectfully traverses these grounds of rejections in view of the following comments.

Sriram in view of Ozluturk

Claims 1, 3, 6-13, and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,366,606 to Sriram (hereinafter "Sriram") in view of U.S. Patent No. 6,366,607 to Ozluturk et al. (hereinafter "Ozluturk"). Of these rejected claims, only claims 1 and 9-12 are independent.

i. Legal Standard

The initial burden of establishing that a claimed invention is *prima facie* obvious rests on the USPTO. *In re Rikckaert*, 9 F.3d 1531, 1532 (Fed. Cir. 1993). To make its *prima facie* case of obviousness, the USPTO must satisfy three requirements:

a) The prior art relied upon, coupled with the knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated to artisan to modify a reference or to combine references. *In re Thrif*, 298 F.3d 1357, 1363 (Fed. Cir. 2002).

b) The proposed modification of the prior art must have had a reasonable expectation of success, and that determined from the vantage point of the artisan at the time the invention was made. *Amgen, Inc. v. Chugai Pharm. Co.*, 927 F.2d 1200, 1209 (Fed. Cir. 1991).

c) The prior art reference or combination of references must teach or suggest all the

limitations of the claims. *In re Vaeck*, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991); *In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, the nature of a problem to be solved. *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999). Alternatively, the motivation may be implicit from the prior art as a whole, rather than expressly stated. *Id.* Regardless if the USPTO relies on an express or an implicit showing of motivation, the USPTO is obligated to provide particular findings related to its conclusion, and those findings must be clear and particular. *Id.*

A critical step in analyzing the patentability of claims pursuant to section 103(a) is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. *See In re Kotzab*, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (*citing In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)). Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher." *In re Kotzab*, 55 USPQ2d at 1316 (*quoting W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983)).

ii. Unique Features of Independent Claims 1 and 9-12

These independent claims 1 and 9-12, in some variation, *inter alia* require a digital processor that can perform both symbol rate processing and at least a portion of the chip rate processing.

In the background of the invention, it is disclosed that a conventional base station has a DSP for performing symbol rate processing and FPGA for performing chip rate processing. The DSP cannot perform the chip rate processing and the FPGA cannot perform the symbol rate processing. When speech is transmitted, the data rate is low but the number of users can be high. Thus, a larger number of FPGAs is needed to perform the chip rate processing on the received speech. That is, the chip rate processing despreads or separates the speech of different users. When transmitting internet data, the data rate is high but the number of users is low. The internet data requires a high number of DSPs so as to perform the symbol rate processing. That is, since the data rate is high, there is more information to decode. The base station is equipped to accommodate both situations: when the number of users is high and when the data transmission rate is high. The two situations, however, will never occur simultaneously. Consequently, unused FPGAs or DSPs are always present in the base station of the conventional techniques (*see* pages 1-2 of the specification).

In an exemplary embodiment of the present invention, however, each digital signal processor can perform the symbol rate processing and the chip rate processing. Thereby, over-dimensioning of the base station is lessened. That is, the digital processor performs both symbol rate processing which is decoding of the received information and at least some of the chip rate processing. The chip rate processing is despreading or re-separating the transmitted information of the different users in the receiver and assigning this information to the different users (*see* page 5, lines 21 to 31 of the specification). In other words, the received data is first despread (separated) and then decoded.

Thereby, when speech is transmitted, more of the processors can be used for the chip rate processing and when Internet data is transmitted, more of the processors can be used for the symbol rate processing. Accordingly, the base station is more compact and resources are used more efficiently. In this base station, a single digital processor despreads as well as decodes the received information. It will be appreciated that the foregoing remarks of an exemplary embodiment relate to the invention in a general sense, the remarks are not necessarily limitative of any claims and are intended only to help the Examiner better understand the distinguishing aspects of the claims mentioned above.

iii. Prior Art References

Sriram discloses a digital transmissions receiver system which includes a digital transmissions receiver and a correlation co-processor. The correlation co-processor performs correlation operations at the request of the digital transmissions receiver. Power consumption in the correlation co-processor is reduced by performing the requested correlation operations in stages. The number of stages used is inversely proportional to the number of gates required to implement the correlation function. Thus, the more stages used, the fewer gates are required. This, in turn, provides lower power consumption as compared with a non-staged implementation of the correlation function. Various types of correlations may be performed as indicated by correlation control signals received from the digital transmissions receiver. A correlation controller, included in the correlation co-processor, keeps track of the various stages and with the data appropriate to each stage. When all of the stages necessary to process a particular piece of data are complete, the recovered symbol rate data is stored in an output buffer to await symbol rate processing by the digital transmissions receiver (col. 1, lines 30 to 55).

In particular, Sriram discloses a digital receiver 10, which is implemented on a DSP (col. 2, lines 31 to 33). The digital receiver 10 interfaces with a programmable correlator co-processor 12, which is a separate unit that communicates with the receiver. The correlator co-processor performs the chip rate processing using a chip correlator 34 (col. 2, lines 49 to 54; col. 3, lines 34 to 50). The DSP (the digital processor) performs the symbol rate processing (Fig. 2; col. 5, lines 51 to 60).

Ozluturk relates to a digital spread spectrum communication system employing pilot-aided coherent multipath demodulation that effects a substantial reduction in global-pilot and assigned-pilot overheads (*see* Abstract). Specifically, Ozluturk discloses a receiver 29 that includes a demodulator 57a, 57b which mixes down the transmitted broadband signal 55 into an intermediate carrier frequency 59a, 59b. A second down conversion reduces the signal to baseband. The QPSK signal is then filtered 61 and mixed 63a, 63b with the locally generated complex pn sequence 43a, 43b which matches the conjugate of the transmitted complex code. Only the original waveforms which were spread by the same code at the transmitter 27 will be effectively despread. Others will appear as noise to the receiver 29. The data 65a, 65b is **then** passed onto a signal processor where FEC decoding is performed on the convolutionally encoded data (Fig. 2; col. 3, lines 41 to 53).

iv. Examiner's Position

The Examiner acknowledges that Sriram fails to disclose or suggest a single processor performing both the chip rate processing and the symbol rate processing (*see* page 2 of the Office Action). The Examiner, however, alleges that Ozluturk cures the deficient teachings of Sriram. Specifically, in response to Applicant's arguments, the grounds of rejection state that, in

Ozluturk, "[t]here are no channel despreaders in the embodiment shown in Fig. 2 and therefore both symbol rate and chip rate processing is performed by the single signal processor 67" (*see* page 6 of the Office Action). The Examiner further notes that Figs. 12 and 13 disclose that symbol rate processing and chip rate processing are performed by the single processing unit 157 (*see* page 7 of the Office Action).

The Examiner further notes that one of ordinary skill in the art would have been motivated to combine the processor of Ozluturk into the system of Sriram "to eliminate the unnecessary circuit components that previously performed the two kind of processing, and thereby save space by making the receiver circuitry more compact" (*see* page 2 of the Office Action).

*v. **Applicant's Position***

Applicant respectfully submits that the USPTO has not established a *prima facie* case of obviousness. The grounds of rejection fail to satisfy the first and third requirements in establishing a *prima facie* case of obviousness. It is respectfully submitted that one of ordinary skill in the art would not have combined the references in the manner suggested by the Examiner without exercising impermissible hindsight. Furthermore, it is respectfully submitted that Ozluturk does not disclose or suggest a single processor performing both the symbol rate processing and at least a part of the chip rate processing.

One of Ordinary Skill in the Art Would Not Have Combined Sriram with Ozluturk without Exercising Impermissible Hindsight

The grounds of rejection note that one of ordinary skill in the art would have been motivated to combine the processor of Ozluturk into the system of Sriram "to eliminate the unnecessary circuit components that previously performed the two kind of processing, and

thereby save space by making the receiver circuitry more compact" (*see* page 2 of the Office Action).

Applicant respectfully submits that neither Ozluturk nor Sriram are directed to eliminating unnecessary components to save space. Sriram relates to reducing power consumption in the correlation co-processor by performing the requested correlation operations in stages. Ozluturk relates to a coherent demodulation system that reduces the air capacity of the global-pilot and assigned-pilot signals while maintaining the desired air-interface performance (col. 2, lines 3 to 6). That is, it is respectfully noted that Ozluturk does not disclose or suggest a more compact device or eliminating circuitry.

On the other hand, page 2, lines 4 to 20 of the specification, clearly disclose the problem of over-dimensioning a receiver and reducing the number of components required for the symbol rate processing and the chip rate processing. In other words, it is Applicant's position that the teachings of the present invention are being used against its teacher. That is, it is respectfully submitted that the grounds of rejection improperly rely on Applicant's disclosure to provide the needed motivation. But for the present invention, one of ordinary skill in the art would not have combined the references in the manner suggested by the Examiner. Accordingly, the combination of Sriram and Ozluturk is a creature of impermissible hindsight. Therefore, the USPTO has not met the first requirement in establishing a *prima facie* case of obviousness.

The Combined Disclosure of Sriram and Ozluturk do not disclose or suggest a processor performing symbol rate processing and at least a portion of chip rate processing

The Examiner concedes that Sriram does not disclose or suggest a processor as claimed in the independent claims 1 and 9-12. The Examiner, however, alleges that Ozluturk cures the deficient teachings of Sriram and discloses a single processor performing both the signal rate

processing and at least a portion of chip rate processing. Specifically, Examiner relies on col. 4, lines 12 to 14 of Ozluturk for meeting these unique features of the independent claims. Col. 4, lines 1 to 15 of Ozluturk recites:

> When the signal is received and demodulated, the baseband signal is at the chip level. Both the I and Q components of the signal are despread using the conjugate of the pn sequence used during spreading, returning the signal to the symbol level. However, due to carrier-offset, phase corruption experienced during transmission manifests itself by distorting the individual chip waveforms. If carrier-offset correction is performed at the chip level, it can be seen that overall accuracy increases due to the inherent resolution of the chip-level signal. Carrier-offset correction may also be performed at the symbol level, but with less overall accuracy. However, since the symbol rate is much less than the chip rate, less overall processing speed is required when the correction is done at the symbol level.

That is, the above-quoted passage of Ozluturk discloses that the carrier offset may be performed at a chip level resulting in increased accuracy or at the symbol level which would result in less processing. In other words, the above-quoted passage of Ozluturk relates to when to determine a carrier offset and not to the chip rate processing and the symbol rate processing. Ozluturk does not disclose or suggest that the chip rate processing is performed by the processor but in the above-quoted passage discusses various pros and cons of performing the offset correction at the chip level and at the symbol level. In short, the above-quoted passage of Ozluturk does not disclose or suggest a processor performing both symbol rate processing and at least a portion of chip rate processing.

Furthermore, with respect to the embodiment of Fig. 2, Ozluturk clearly discloses that the receiver 29 includes a demodulator 57a, 57b which mixes down the transmitted broadband signal 55 into an intermediate carrier frequency 59a, 59b. A second down conversion reduces the signal to baseband. The QPSK signal is then filtered 61 and mixed 63a, 63b with the locally generated complex pn sequence 43a, 43b which matches the conjugate of the transmitted complex code. Only the original waveforms which were spread by the same code at the transmitter 27 will be effectively despread. Others will appear as noise to the receiver 29. "The data 65a, 65b is then passed onto a signal processor 59 where FEC decoding is performed on the convolutionally encoded data" (col. 3, lines 42 to 53). That is, the signal processor receives despread digital data 65a and 65b for FEC decoding.

In other words, in Ozluturk, the signal is despread prior to being input into the signal processor 59/67. That is, chip rate processing is not performed by the digital processor but is performed prior to the signals reaching the digital processor. Moreover, in Ozluturk, the signal processor 59/67 only performs forward error correction (FEC), which is decoding of the encoded data (col. 3, lines 51 to 53). Ozluturk, similar to the conventional technique's described in the background of the invention and Sriram, discloses a receiver with a signal processor for performing only the symbol rate processing (Fig. 2), whereas the chip rate processing is performed by elements such as channel despreaders (depicted as elements 43a and 43b in Fig. 2) prior to the decoding by the signal processor. In short, Ozluturk is no different from the processor disclosed in Sriram or from the processor disclosed in the background of the invention and as such clearly fails to cure the deficient teachings of Sriram.

The grounds of rejection further allege that the embodiment depicted in Figs. 12 and 13 of Ozluturk disclose the unique features of these independent claims (*see* page 7 of the Office Action). Applicant respectfully submits that Fig. 12 of Ozluturk clearly shows the symbols entering the processor 157. That is, the chip rate processing has already been performed to return the signals to their symbol state *i.e.*, prior to the symbols entering the processor 157. For example, the signals have been despread by the despreaders 85_1 to 85_n depicted in Figs. 11 and 13 (col. 6, lines 38 to 65 and col. 7, lines 25 to 30).

Therefore, a digital processor that can perform both symbol rate processing and at least a portion of the chip rate processing, as set forth in some variation in the independent claims 1 and 9-12 is not suggested by the combined teachings of Sriram and Ozluturk, which lack having a digital processor execute at least a portion of the chip rate processing. Therefore, the USPTO has not met the third requirement in establishing a *prima facie* case of obviousness.

Concluding Remarks

In summary, Applicant respectfully submits that one of ordinary skill in the art would not have been motivated to combine the references in the manner suggested by the Examiner without exercising impermissible hindsight. Furthermore, The combined disclosures of Sriram and Ozluturk do not suggest the unique features of claims 1 and 9-12 discussed above. Ozluturk despreads the signals *i.e.*, performs the chip rate processing, prior to providing them to the processor, which only performs the symbol rate processing. For at least these exemplary reasons, claims 1 and 9-12 are patentable over Sriram in view of Ozluturk. Accordingly, Applicant respectfully requests the Examiner to withdraw this rejection of claims 1 and 9-12. Claims 3, 6-8, 13, and 19 are patentable at least by virtue of their dependency on claim 1 or 12.

Sriram in view of Ozluturk and Warty

Claims 2, 14, and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram and Ozluturk in view of U.S. Patent No. 4,827,499 to Warty (hereinafter "Warty"). Applicant respectfully traverses this rejection in view of the following comments.

Of these rejected claims 2, 14, and 16, claim 2 depends on claim 1 and claims 14 and 16 depend on claim 12. Applicant has already demonstrated that the combined teachings of Sriram and Ozluturk fail to teach or suggest a digital signal processor configured to perform a symbol rate processing and at least parts of a chip rate processing. Warty is cited only for its teachings of processors performing task allocation (*see* page 4 of the Office Action). Clearly, Warty does not cure the deficient teachings of Sriram. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claims 1 and 12. Since claims 2, 14, and 16 dependent upon claim 1 or 12, they are patentable at least by virtue of their dependency.

Sriram in view of Ozluturk, Warty, and Komara

Claims 4, 5, and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram, Ozluturk and Warty in view of U.S. Patent No. 6,161,024 to Komara (hereinafter "Komara"). Applicant respectfully traverses this rejection in view of the following comments.

Of these rejected claims 4, 5, and 15, claims 4 and 5 depend on claim 1 and claim 15 depends on claim 12. Applicant has already demonstrated that the combined teachings of Sriram, Ozluturk, and Warty fail to teach or suggest a digital signal processor configured to perform a symbol rate processing and at least parts of a chip rate processing. Komara is only

cited for its teachings of a group of digital processors (*see* page 5 of the Office Action). Clearly, Komara does not cure the deficient teachings of Sriram, Ozluturk, and Warty.

Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved the subject matter of claims 1 and 12. Since claims 4 and 5 depend on claim 1 and claim 15 depends on claim 12, they are patentable at least by virtue of their dependency.

Ozluturk in view of Subramanian

Claims 20-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozluturk in view of a newly cited U.S. Publication No. 2001/0034227 to Subramanian et al. (hereinafter "Subramanian"). Applicant respectfully traverses these grounds for a rejection in view of the following comments.

First, it is respectfully noted that claims 22 and 23 cannot be obvious over Ozluturk and Subramanian and this rejection is improper. Claims 22 and 23 depend on claim 1 and as such contain all the features of claim 1. If the Examiner deemed necessary to reject claim 1 as being obvious over Sriram in view of Ozluturk (that is, Sriram is necessary to meet the unique features of claim 1). Accordingly, claims 22 and 23 should have been rejected as being obvious over Sriram, Ozluturk, and Subramanian.

It is respectfully submitted that Subramanian is being cited only for its disclosure of the switching means (*see* page 5 of the Office Action). Clearly, Subramanian does not cure the deficient teachings of Sriram, and Ozluturk. Together, the combined teachings of these references would not have (and could not have) led the artisan of ordinary skill to have achieved

the subject matter of claim 1. Since claims 22 and 23 depend on claim 1, they are patentable at least by virtue of their dependency.

Of the remaining rejected claims 20, 21, and 24, only claim 20 is independent. Independent claim 20 *inter alia* recites: "means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing, wherein the digital signal processor is a single digital processor having the symbol rate processing means, the chip rate processing means and the switching means and wherein the digital signal processor is disposed inside a receiver." As explained above, Ozluturk does not disclose or suggest a single processor having means for executing chip rate processing and means for executing symbol rate processing. Subramanian is cited only for its disclosure of switching and as such does not cure the deficient disclosure of Ozluturk.

That is, Subramanian relates to a method of generating a configuration for a configurable spread spectrum communication device. The method is implemented on a computing device and starts with receiving an input identifying a desired function, and a desired operation within the desired function, to be implemented by a configurable communication device. Subsequently, a signal flow path for the desired operation is generated by the computing device. Next, the desired operation is mapped onto a computing element within the configurable communication device; the computing element having localized control and being function-specific. The configurable device is configured to enable the mapping operation and signal flow path across a computing element for each of the multiple operations which together enable the desired function (*see* Abstract and ¶¶ 9 through 11).

That is, Subramanian discloses a complex computing device which generates a signal flow path and maps it onto various configurable elements of the configurable device. This computing device needs its own processor, memory and user interface. In other words, Subramanian does not disclose or suggest having a single processor perform the chip rate processing, the symbol rate processing, and the switching. In Subramanian, a separate computing device with a memory and a user interface is provided to map out the signal flow (element 102 in Fig. 1A and Fig. 2; ¶¶ 21 and 30). Then, the mapped out signal flow is transferred to the configurable device 104 for implementation (Fig. 1; ¶¶ 22 and 24). In other words, Subramanian clearly discloses separate devices for the spread spectrum processing and for the switching. Subramanian does not cure the deficient disclosure of Ozluturk.

Moreover, one of ordinary skill in the art would not have been motivated to combine the references, in the manner suggested by the Examiner. The Examiner contends that one of ordinary skill in the art would have been motivated to combine the references for most effective processing based on the type of processing required at any given time (*see* page 5 of the Office Action).

However, in Ozluturk, separate elements are provided for the symbol rate processing and the chip rate processing. In Ozluturk, there is no need to having a switch for switching between the two. That is, since separate elements are provided for each type of processing, these processes can be performed concurrently and the switch is not needed. Moreover, in Ozluturk, there is no disclosure or suggestion that some of the elements should be bypassed. Therefore, the proposed combination would not provide a more effective processing. Furthermore, the proposed combination results in an unworkable combination. A computing device of

Subramanian (with the memory, the processor, and the user interface) cannot be placed in the processor of Ozluturk. In short, one of ordinary skill in the art would not have combined the two references in the manner suggested by the Examiner.

Therefore, "means for switching over from said means for executing symbol rate processing to said means for executing chip rate processing, wherein the digital signal processor is a single digital processor having the symbol rate processing means, the chip rate processing means and the switching means and wherein the digital signal processor is disposed inside a receiver," as set forth in claim 20 is not obvious in view of the combined teachings of Ozluturk and Subramanian, which lack a single processor having the symbol rate processing means, the chip rate processing means, and the switching means. For at least these exemplary reasons, independent claim 20 is patentable over Ozluturk in view of Subramanian. Accordingly, Applicant respectfully requests the Examiner to withdraw this rejection of claim 20 and its dependent claims 21 and 24.

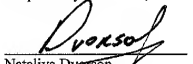
Furthermore, with respect to the dependent claim 24, the Examiner contends that one of ordinary skill in the art would have been motivated to combine the references to ensure that the processing is matched to the appropriate sources (*see* page 6 of the Office Action). This motivation is not understood. It is respectfully requested that the Examiner further clarify what is meant by "the appropriate sources."

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860
WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Nataliya Dvorson
Registration No. 56,616

Date: November 6, 2006

Attorney Docket No.: Q66664